Lab 4 Writeup: The PLL

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Abstract

In lab 4 a LM565 Phase-locked-loop (PLL) was built to act as the demodulator of our intermediate $300kHz$ FM output of the mixer on our receiver. The chip and design worked well, with $> \pm 170kHz$ hold range and a minimum detectable input signal of $10mV$. The PLL also sounded great, with $THD < 1\%$ for an input $1kHz$ modulating signal with $\Delta f = 50kHz$. A block diagram of the basic function of the PLL along with the components I chose is shown in Figure 1, below.

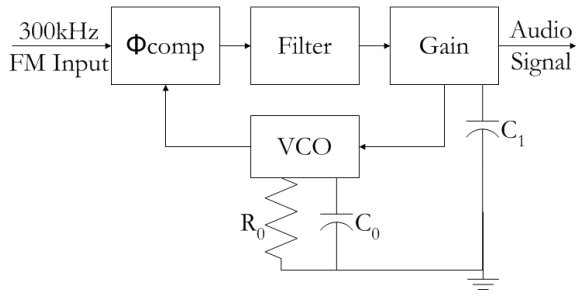

Figure 1: Lab 4 Block Diagram

1 PLL Design Specifications

The PLL designed is used to demodulate the $300kHz$ intermediate frequency FM signal from the output of the SA612 mixer on the receiver into a baseband audio signal, and is thus the last block before the human ear (or an audio amp). Because our transmitter is sending FM with $\Delta f = 50kHz$, our PLL needs to be able to lock onto frequencies in the $250kHz - 350kHz$, and preferably a much larger range, as the discrete colpitts center frequency on the transmitter is rarely right on $24.3MHz$. To meet these needs, a PLL with the below specifications was designed using the LM565 chip.

- Supply Rails: 9V and OV
- Free Running Frequency (f_0): $300kHz$
- Hold Range (f_h): $> \pm 50kHz$
- Loop Bandwidth (f_n) : $> 100kHz$

2 Design Theory

What is a phase-locked loop? At the basic level, it is the inverse of a VCO–a PLL outputs a voltage that is a function of input signal frequency. In essence, a PLL is a VCO with a feedback loop designed so that the VCO can replicate the incoming signal frequency. This feedback loop involves a phase comparator (multiplier), a low-pass integrator, and a gain stage.

The multiplier takes the square wave VCO output and the input signal and outputs a series of pulses whose widths are dependent on the frequency offset between these signals. These pulses are integrated into a DC signal via the filter and amplified in the gain stage. The DC signal is used as the control voltage for the VCO block. In sum, the feedback loop locks the VCO to the incoming frequency by using the error voltage (difference in frequency) to control the VCO.

By inputting a varying frequency signal, this error voltage, which is the PLL output and VCO control voltage, will change in proportion to the varying frequency. We have a simple FM demodulator!

Now, in order to get a PLL to meet our design specifications, we need to configure both the filter characteristics and the center frequency of the VCO. The below equations, from the LM565 datasheet, describe how to do this.

$$f_0 = \frac{0.3}{R_0 C_0} \tag{1}$$

$$LoopGain = K_0 K_D = \frac{33.6 f_0}{V_c} \tag{2}$$

$$f_h = \pm \frac{8}{V_c} \tag{3}$$

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_0 K_D}{R_1 C_1}} \tag{4}$$

2.1 Final Design

In (1), we set the center frequency of the VCO using timing resister R_0 and capacitor C_0. To get $f_0 = 300kHz$ this equation yields values of $10k\Omega$ and $100pF$. To assure reaching this free-running frequency, I decided to use a $100k\Omega$ potentiometer for R_0.

In (3), we can see if we have met our hold range constraint. In deed, with the above R_0 and C_0 and $V_c = 3v$, (3) results in a range of $f_h = \pm 267kHz$, well more than enough.

In (4) we use the loop gain calculated in (2) to set the capacitor C_1 in our low-pass filter. Using a $330pF$ for C_1 and doing the math yields $f_n = 155kHz$ in the acceptable range.

3 LAB Results

A PLL with the values calculated in the above section was built in lab and found to use $72mW$ of power. I will now go on to describe its more interesting operating characteristics.

3.1 Hold Range

First, lets discuss the predictable behavior of the PLL. When the input frequency is equal to the free running f_0 of the PLL, we expect the VCO output to be 90° out of phase with the input, as it is in the middle of the PLL lockable frequency range. Likewise at the boundaries of the PLL lockable range, we expect to see phase differentials of 0° and 180°. The below three figures show these three cases. For reference, in each plot the VCO output is the squarewave.

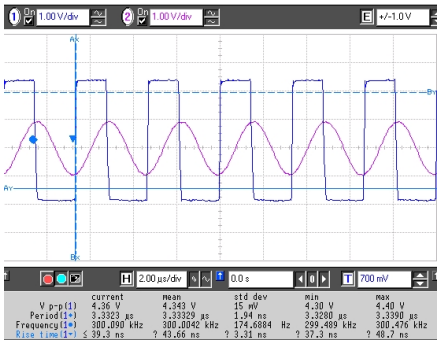

Figure 2: At $f_in = f_0 = 300kHz$

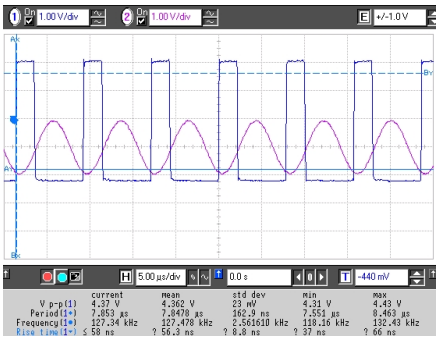

Figure 3: At $f_in = f_0 - f_h \approx 127kHz$

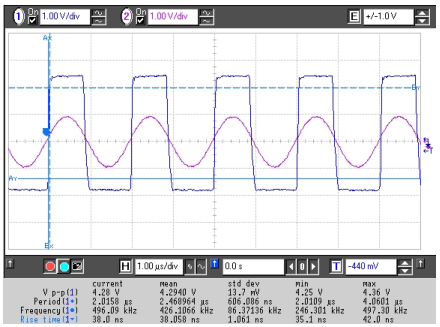

Figure 4: At $f_in = f_0 + f_h \approx 496kHz$

As the figures indicate, the PLL is operating according to these principles. I am uncertain why the duty cycle is different for the VCO in the $f_0 - f_h$ case, though if you look at the downward edge of the square wave, you can see it occurs 180° out of phase, as I expected. Of note is that this range is certainly less than the $\pm 267kHz$ predicted by the datasheet equations, which in some ways is good, because we really don't need that much bandwidth.

To test equation (3) these minimum and maximum lockable frequencies were also found for $V_c = 16V$. At $16V$ they were $170kHz$ and $431kHz$ respectively–i.e. f_h was $130kHz$. Equation 3 predicted $f_h = 150kHz$, so overall, these findings were pretty close to the datasheet prediction.

3.2 Sensistivity

Next, we can look at the linearity of the PLL–i.e., how linearly the output voltage changes with input frequency. This is crucial to get a non-distorted demodulated signal. Figure 5 shows the PLL's very linear sensitivity k in $\frac{mV}{kHz}$.

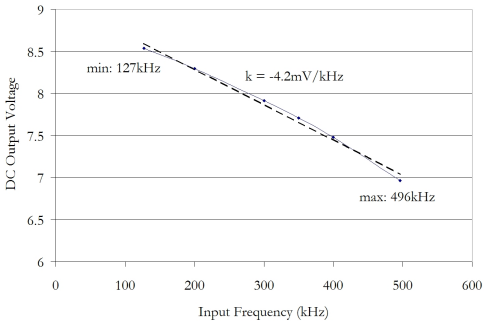

Figure 5: PLL k ($\frac{mV}{kHz}$)

3.3 Overall Performance

Figure 6 shows the PLL output of a test $1V, 1kHz$ modulating signal with $\Delta f = 50kHz$ and center frequency $f_c = 300kHz$. A triangle-like $1kHz$ wave is visible beneath all the noise, I promise.

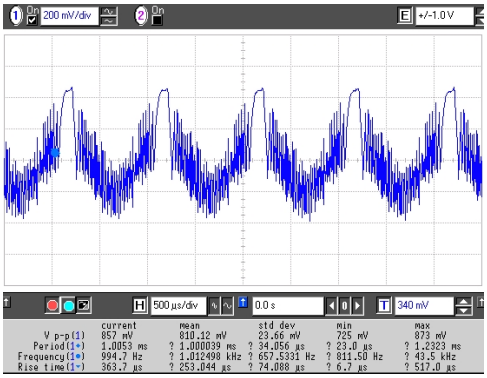

Figure 6: Noisy 1kHz PLL output

Though this output may look ugly, when I viewed it on the low frequency spectrum analyzer, the picture (from $500Hz - 20kHz$) was much prettier. The fundamental $1kHz$ tone showed up at $-17dB$, and all the other signal harmonics are $-60dB$ or below. It seems that much of the noise is well away from audible frequencies, likely $300kHz$ feed-through and possibly even $24MHz$ crystal noise feed-through as well. However, both of these frequency components are inconsequential, for the ear picks up neither of them. In the audible frequency ranges, the PLL output was clean with $1\%THD$.

3.4 Transmitting

With the final crucial block of my receiver in place, I was able to transmit and receive un-aided by spectrum-analyzer Demod functions. Using antennas, my discrete colpitts transmitter, and the LNA and mixer on my receiver, I was able to successfully transmit across the LAB with very good audio quality, much better than the AM peak detector from lab 1. My minimum detectable signal direct-connected from the RF generator to my LNA was $-85dBm$ and $-50dBm$ when directly connected to my multiplier input. This difference shows both the benefits of the LNA and the negative impacts of the mismatch between the RF generator 50Ω output impedance and the $1.5k\Omega$ mixer input impedance.

4 Conclusion

A PLL was implemented using the LM565 chip to have a free running frequency of $300kHz$ and a bandwidth wide enough to successfully demodulate our transmitted signals. It used 72mW of power and provided signals with $1\%THD$ in the audio frequency range. I feel that once I have the IF and power amps in place my transmitter-receiver will be poised to be a rather effective combination.